Remarks

This amendment is in response to the Office Action dated November 8, 2002. Claims 1-4 and 9-13 have been amended and new claim 24 has been added. Claims 5, 7 and 14-23 have been canceled without prejudice. Claims 1-4, 6, 8-13 and 24 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 14-23 were canceled without prejudice as non-elected claims.

Applicant has amended the specification as requested by the Examiner by inserting the application numbers for the two co-pending applications listed one page 1 of the specification.

Claims 1-13 were "provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-11 of copending application No. 09/963,903." Applicant notes that the present application is no. 09/963,903. Applicant is unsure which application the Examiner is referring to. Applicant notes that application nos. 09/963,168 and 09/963,924 were incorporated by reference into the present application. If the Examiner is referring to one of these cases, applicant respectfully submits that the claims of the present application include aspects not recited in the claims of these cases. For example, claim 1 of the present application, as amended, recites in part "forming a second insulation layer that fills the recessed section on the second conductive layer, the second insulation layer comprising a material different from that of the first insulation layer". Such a feature does not appear in claims 1-11 of either of the other two cases. Accordingly, applicant respectfully requests that the rejection be withdrawn.

Claims 1-13 were rejected under 35 U.S.C. 112, second paragraph. Applicant does not agree with the Examiner that the terms "conduction layer" are indefinite. However, to expedite prosecution, applicant has amended the claims to replace "conduction" with "conductive" as suggested by the Examiner. Applicant has also amended several other elements of claim 1 for clarity. For claim 2, applicant does not agree that the terms "more difficult to etch" are indefinite. However, to expedite prosecution, applicant has deleted those terms and amended the claim to recite "more resistant to an etchant". For Claim 4, applicant has deleted the terms "the first through hole is continuous to" and amended the claim to recite that "the second through hole overlaps the first through hole." The Examiner stated for claims 10-11 that the terms "ion

implantation operation" are used. However, it does not appear that such terms are in the claims. In view of the above, applicant respectfully submits that claims 1-13 comply with section 112.

Claims 1-4, 6 and 9-13 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,960,270 to Misra et al. (hereinafter "Misra"). The rejection is respectfully traversed.

Applicant does not agree with the Examiner's characterization of Misra.

First, the Examiner cited Misra Fig. 16 and col. 10, line 1-16 in an effort to establish that Misra describes "removing a part of the first conduction layer in a manner so that the gate dielectric layer is not exposed to thereby form a recessed section on the first conduction layer between the insulating layers." Office Action at page 6. Applicant notes that the Examiner referred to Misra reference number 108 as a "first conduction layer"(please note that Misra at col. 10, line 3, appears to erroneously use reference number 110 to refer to layer 108). As seen in Misra Fig. 16, the entire layer 108 is removed, thus exposing the layer 106. Layer 106 in Misra is referred to in Misra col. 10, line 7 as a gate oxide and is the remaining part of layer 105 (See Fig. 10), which the Examiner referred to as a gate dielectric layer. The Examiner stated at page 6 of the Office Action that Misra at col. 10, lines 1-16 describes "not exposing the gate oxide 125". However, the Examiner already referred to layer 105 (and thus 106) as the gate dielectric layer for purposes of the proposed rejection. As seen in Misra Fig. 16, the gate oxide 106 is exposed. As stated in Misra at col. 10, lines 11-13, the layer 125 may be formed after the layer 108 has been removed. Moreover, as stated in Misra at col. 10, lines 14-15, the layer 106 may comprise all or part of layer 125. Thus, the Examiner's citations to Misra appear to describe a method where the conductive layer 108 is removed and the gate oxide 106 is exposed. Thus, applicant respectfully submits that the Examiner has cited no portion of Misra that describes or suggests "removing a part of the first conductive layer in a manner that the gate dielectric layer is not exposed to thereby form a recessed section on the first conductive layer between the sidewall insulation layers" as recited in claim 1.

The Examiner further cited Figs. 19-22 in an effort to establish that Misra describes "filling a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer." Office Action at page 6. As noted by the Examiner, the steps in Figs. 10-16 of Misra are also used in the embodiment described in Figs. 19-22. The Examiner referred to Misra reference number 108 as a "first

conduction layer". As seen in Misra Fig. 16, the entire layer 108 is removed. Fig. 19 shows layer 129, which is a different layer from layer 108. The layer 108, which the Examiner referred to as the first conduction layer, appears to no longer exist when the layer 129 is formed. Thus, applicant respectfully submits that the Examiner cited no portion of Misra that describes "partially filling the recessed section with a second conductive layer to form a gate electrode that includes at least the first conductive layer and the second conductive layer forming a second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer" as recited in claim 1.

The Examiner further stated on page 6 of the Office Action that Misra discloses "forming a second insulation layer at the recessed section on the second conduction layer, the second insulation layer being composed of a material different from that of the first insulation layer (Misra fig. 14 # 120 of nitride the first insulating layer of oxide)." Applicant notes that earlier on page 6 of the Office Action, the Examiner appeared to refer to Fig. 14 and reference number 120 of Misra as the "first insulation layer covering the first conductive layer and the side wall spacers." Thus, applicant does not understand the Examiner's use of the same reference number for both the first and the second insulating layers. Accordingly, applicant respectfully submits that the Examiner has cited no portion of Misra that describes "forming a second insulation layer that fills the recessed section on the second conductive layer, the second insulation layer comprising a material different from that of the first insulation layer" as recited in claim 1.

The rejection of dependent claims 2-4 and 6 should be withdrawn for at least the same reasons as claim 1. Moreover, as it is unclear which layers the Examiner is referring to as a first and second insulation layers, the Examiner specific rejections of dependent claims 2, 4 and 6 are also unclear and should be withdrawn for this reason in addition to the reasons stated above for claim 1. In addition, for claim 3, the Examiner cited the presence of layer 108 and then cited Misra col. 10, lines 42-45 and 57-60 for "the steps of depositing a metal layer for siliciding the first conduction layer, on the first conduction layer" and for "siliciding the first conduction layer to form a silicide layer." However, applicant notes that Misra col. 10, lines 42-45 and 57-60, appears to refer to the embodiment illustrated in Figs. 19-22. As stated earlier, the layer 108 appears to have been completely removed prior to deposition of any additional layers shown in Figs. 19-22. As a result, there is no depositing a metal layer on the first conduction layer as

suggested by the Examiner. Accordingly, for at least this reason in addition to the reasons stated above for claim 1, the rejection of claim 3 should be withdrawn.

Claim 9 and its dependent claims 10-13 can be distinguished for at least some of the same reasons discussed above.

Claims 5 and 7 were rejected under 35 U.S.C. 103(a) over Misra in view of U.S. Patent No. 6,465,359 to Yamada. This rejection has been rendered moot as these claims have been canceled without prejudice.

New dependent claim 24 was added. Support for the claim may be found throughout the specification and in the original claims. It is believed that no new matter has been entered. Examination is respectfully requested.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-4, 6, 8-13 and 24 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes

Alan S. Raynes **March 10 , 2003**
(Date)

Version With Markings to Show Changes Made

The paragraph at page 1, lines 6-11 was amended as follows:

Applicant hereby incorporates by reference Japanese Application No. 2000-292142, filed September 26, 2000, in its entirety. Applicant hereby incorporates by reference U.S. Application Serial No. 09/963,168 [_____], filed September 26, 2001, [listing Yoshikazu Kasuya as inventor, having docket number 15.47/6065,] in its entirety. Applicant hereby incorporates by reference U.S. Application Serial No. 09/963,924 [_____], filed September 26, 2001, [listing Yoshikazu Kasuya as inventor, having docket number 15.49/6067,] in its entirety.

Claims 1-4 and 9-13 were amended as follows:

1. (amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

(b) forming a gate dielectric layer on a semiconductor layer;

(b) forming a first [conduction] conductive layer having a specified pattern on the gate dielectric layer;

(c) forming sidewall insulation layers on side walls of the first [conduction] conductive layer;

(d) forming a source region and a drain region in the semiconductor layer;

(e) depositing a first insulation layer that covers the first [conduction] conductive layer and the sidewall insulation layers, the first insulation layer comprising a material different from that of the sidewall insulation layers;

(f) planarizing the first insulation layer until an upper surface of the first [conduction] conductive layer is exposed;

(g) removing a part of the first [conduction] conductive layer in a manner that the gate dielectric layer is not exposed to thereby form a recessed section on the first [conduction] conductive layer between the sidewall insulation layers;

(h) partially filling the recessed section with a second [conduction] conductive layer [in the recessed section] to form a gate electrode that includes at least the first [conduction] conductive layer and the second [conduction] conductive layer;

(i) forming a second insulation layer that fills [at] the recessed section on the second [conduction] conductive layer, the second insulation layer [being composed of] comprising a material different from that of the first insulation layer;

(j) etching the first insulation layer to form a first through hole that reaches the source region or the drain region; and

(k) forming a first contact layer in the first through hole.

2. (amended) A method for manufacturing a semiconductor device according to claim 1, wherein, in the step (j), the second insulation layer and the sidewall insulation layers [are composed of] comprise a material that is more [difficult to etch] resistant to an etchant than the first insulation layer.

3. (amended) A method for manufacturing a semiconductor device according to claim 1, wherein the first [conduction] conductive layer is a silicon layer, and the step (h) includes the steps of

(h – 1) depositing a metal layer for siliciding the first [conduction] conductive layer on the first [conduction] conductive layer; and

(h – 2) siliciding the first [conduction] conductive layer to form a silicide layer.

4. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising:

(l) forming a third insulation layer on the first insulation layer and the second insulation layer;

(m) etching the third insulation layer to form a second through hole; and

(n) forming a second contact layer in the second through hole, wherein [the first through hole is continuous to] the second through hole overlaps the first through hole.

9. (amended) A method for manufacturing a semiconductor device, comprising:

forming a gate dielectric layer on a semiconductor layer;

forming a first [conduction] conductive layer having a specified pattern on the gate dielectric layer;

forming sidewall insulation layers on side walls of the first [conduction] conductive layer;

forming a source region and a drain region in the semiconductor layer;

removing a part of the first [conduction] conductive layer in a manner so that the gate dielectric layer is not exposed, to thereby form a recessed section on the first [conduction] conductive layer between the sidewall insulation layers, wherein the removing a part of the first [conduction] conductive layer is carried out after formation of the source region and the drain region;

forming a second [conduction] conductive layer in a portion of the recessed section; and

forming an insulation layer in the recessed section on the second [conduction] conductive layer.

10. (amended) A method for manufacturing a semiconductor device according to claim 9, further comprising, after forming the source region and the drain region and before removing a part of the first [conduction] conductive layer:

forming a first insulating layer that covers the first [conduction] conductive layer, the sidewall insulation layers, and the semiconductor layer; and

planarizing the first insulation layer so that the first [conduction] conductive layer is exposed.

11. (amended) A method for manufacturing a semiconductor device according to claim 10, further comprising, after forming the insulation layer in the recessed section above the second [conduction] conductive layer:

etching the first insulation layer to form a first through hole that reaches the source region or the drain region; and

forming a first contact layer in the first through hole.

12. (amended) A method for manufacturing a semiconductor device according to claim 9, wherein the second [conducting] conductive layer comprises a silicide.

13. (amended) A method for manufacturing a semiconductor device according to claim 9, wherein the removing a part of the first [conduction] conductive layer further includes removing a greater depth of the first [conduction] conductive layer from a center region than from end regions adjacent to the sidewall insulation layers.